

REMARKS

Claims 1 through 17 are pending in this application, of which claims 6 through 7 stand withdrawn from consideration pursuant to the provisions of 37 C.F.R. §1.142(b). Accordingly, claims 1 through 5 are active.

Claims 1 through 5 were rejected under 35 U.S.C. §103 for obviousness predicated upon the acknowledged prior art (Fig. 1D and the related discussion thereof) in view of Gates et al.

In the statement of the rejection, the Examiner made clearly inaccurate factual determinations as to the teachings of the acknowledged prior art, notably, Fig. 1D and the related discussion thereof in the written description of the specification, and then conclude that one having ordinary skill in the art would have been motivated to modify the acknowledged prior art in view of Gates et al. This rejection is traversed.

The Examiner's determinations as to the teachings of the acknowledged prior art involves several clear factual inaccuracies. Firstly, the Examiner referred to Fig. 1D, asserting that reference numeral 1 denotes a via plug. This is inaccurate. Reference numeral 1 does not denote a via plug. Rather, as specifically set forth on page 2 of the written description of the specification, lines 14 through 17, reference numeral 1 denotes a **lower layer interconnect line**. An **interconnect line**, as one having ordinary skill in the art would have understood, **is not a via plug**.

Rather, as clearly disclosed at page 3 of the written description of the specification, lines 22 through 26, reference numeral **7B is a via plug**, while the upper layer interconnect line is denoted by reference numeral 8B, as accurately noted by the Examiner.

In addition, the Examiner's clearly inaccurate factual determination that spells death to the imposed rejection is the attempt to read claim 1 on the relative position of the etching stopper 5 and the metal interconnect 8B as set forth in the penultimate paragraph on page 2 of the March 25, 2005 Office Action. Specifically, independent claim 1 requires the upper surface of the etching stopper to be located under the upper surface level of the metal interconnect line and, significantly, independent claim 1 further requires that "...the under surface of said etching stopper is located over the undersurface level of said metal interconnect." This quoted claim limitation from claim 1 is **not** satisfied by the acknowledged prior art semiconductor device depicted in Fig. 1D. This is because in Fig. 1D, the undersurface of the etching stopper 5 is clearly located **under**, repeat **under**, the undersurface of the metal interconnect 8B-not not **over** the undersurface level of the metal interconnect as specified in claim 1.

In view of the above significant structural differences between the claimed semiconductor device and the acknowledged prior art semiconductor device, it is apparent that even **if** the acknowledged prior art device is modified as proposed by the Examiner in view of Gates et al., and Applicants do **not** agree that the requisite fact-based motivation has been established, the claimed invention would **not** result. *Uniroyal, Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988).

Applicants, therefore, submit that the imposed rejection of claims 1 through 5 under 35 U.S.C. §103 for obviousness predicated upon the acknowledged prior art in view of Gates et al. is not factually or legally viable and, hence, solicit withdrawal thereof.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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